WHAT IS CLAIMED IS:

1. A system for allowing shared access by at least two processors including an embedded controller and a host processor to at least two modules comprising:

at least two modules; and

a transaction control;

wherein the embedded controller is capable of providing an indication of which of the at least two modules to access to said transaction control; and

the host processor is capable of providing an indication of which of the at least two modules to access to said transaction control.

2. The system of claim 1, further comprising:

at least one access block bit controlled by one of the at least two processors for blocking access by another of the at least two processors to at least one of the at least two modules.

3. The system of claim 2, wherein said at least one access block bit is capable of enabling at least one of the at least two modules.

4. The system of claim 1, further comprising:

a bus extension, wherein at least one of the at least two modules is accessible via said bus extension; and

wherein said transaction control is capable of providing to said bus extension an indication of said at least one of the modules, accessible via said bus extension, for access by the host processor;

said transaction control is capable of providing to said bus extension an indication of said at least one of the modules, accessible via said bus extension, for access by the embedded controller;

and said bus extension is capable of providing an indication of said at least one of the modules for access by one of the processors.

5. The system of claim 1,wherein said transaction controlis capable of providing an indication of at least one of the at least two modules for access by one of the processors.

6. The system of claim 1, wherein at least one of the at least two modules is part of an input/output chip.

7. A system for allowing shared access by at least two processors including an embedded controller and a host processor to at least one module, comprising:

a main power supply;

an alternative power supply;

at least one module, wherein at least part of the at least one module is powered by said alternative power supply;

one internal bus connected to both said at least part of the at least one module which is powered by said alternative power supply and to at least part of at least one module which is powered by said main power supply; and

at least one processor interface powered by said alternative power supply;

wherein at least one of the at least two processors is capable of accessing through said one bus said at least part of the at least one module which is powered by said alternative power supply, even when said main power supply is off.

8. The system of claim 7, further comprising:

a domain separator for isolating said at least part of at least one module which is powered by the main power supply from the at least part of the at least one module powered by the alternative power supply, when the main power supply is off.

9. The system of claim 7, further comprising:

a main power on detect circuit capable of detecting if the main power supply is within specified active range.

10. The system of claim 7, further comprising:

an alternative power up reset;

a main power up reset; and

a generator generating a reset select signal;

wherein said reset select signal is capable of selecting between an alternative power up reset and a main power up reset for resetting at least one bit powered by the alternative power supply within the at least one module at least partially powered by the alternative power supply.

11. The system of claim 10, wherein said at least one bit powered by the alternative power supply is a content lock bit.

12. The system of claim 11, wherein said content lock bit at least locks itself, further comprising:

at least one unlock bit for resetting said at least one content lock bit.

13. The system of claim 12, wherein said at least one unlock bit is controlled by said at least one processor whose interface is powered by the alternative power supply.

14. The system of claim 10, wherein said generator for generating said reset select signal is at least one reset select bit.

15. The system of claim 14, wherein said at least one reset select bit is controlled by the at least one processor whose interface is powered by said alternative power supply.

16. The system of claim 7, wherein the at least one module is part of an input/output chip.

17. The system of claim 7, further comprising an extension bus powered by the alternative power supply;

wherein the at least one module is accessed via said extension bus.

18. A system for allowing shared access by at least two processors including an embedded controller and a host processor to at least one module, comprising:

at least one module;

at least one access block bit controlled by one of the at least two processors for blocking access by another of the at least two processors to the at least one module;

at least one access block violation flag bit capable of providing an indication to said one of the at least two processors if said another processor attempts access to the at least one module whose access has been blocked; and

circuitry for providing to said another of the at least two processors an indication that said at least one access block bit is set to block access.

19. The system of claim 18, wherein said circuitry is capable of providing said indication to said another of the at least two processors if said another processor attempts access to the at least one module whose access has been blocked.

20. The system of claim 19, wherein said indication to said another of the at least two processors is an error indication.

21. The system of claim 19, wherein said indication to said another of the at least two processors is a not ready indication.

22. The system of claim 18, further comprising at least one activation bit for the at least one module, wherein said indication is provided to said another of the at least two processors when said another processor reads said at least one activation bit.

23. The system of claim 22, further comprising at least one activation status configuration bit controlled by said one of the at least two processors, wherein said activation status configuration bit is capable of controlling whether said indication is provided when said another processor reads said at least one activation bit.

24. The system of claim 18, wherein said at least one access block bit is capable of enabling the at least one module.

25. The system of claim 18, further comprising a bus extension, wherein said at least one module is accessible via said bus extension.

26. The system of claim 18, wherein said at least one module is part of an input/output chip.

27. A system for allowing shared access to at least one module by at least two processors including an embedded controller and a host processor, comprising:

at least one module; and

at least one access block bit controlled by one of the at least two processors, wherein said at least one access block bit is capable of blocking access to the at least one module by another of the at least two processors and is capable of enabling the at least one module.

28. The system of claim 27, wherein said at least one access block bit is also capable of enabling an output of the at least one module.

29. The system of claim 27, further comprising:

at least one disable bit controlled by said one of the at least two processors, wherein said at least one disable bit is capable of disabling the at least one module even if said at least one access block bit is set to enable said at least one module.

30. The system of claim 27, further comprising:

at least one tri-state bit controlled by said one of the at least two processors, wherein said at least one tri-state bit is capable of disabling said output of the at least one module even if said at least one access block bit is set to enable said output of the at least one module.

31. The system of claim 27, wherein the at least one module is part of an input/output chip.

32. A system for allowing concurrent access to at least one module by at least two processors including an embedded controller and a host processor, comprising:

at least one module; and

access control circuitry included in the at least one module wherein said access control circuitry is capable of regulating access within the at least one module by the at least two processors, thereby allowing concurrent access.

33. The system of claim 32, wherein the at least one module further includes:

a separate index register within the at least one module, corresponding to each of the at least two processors.

34. The system of claim 33 wherein said access control circuitry only allows access to said separate index register by said corresponding processor.

35. The system of claim 33, wherein the at least one module further includes at least one internal register; and

said access control circuitry only allows access by each of said at least two processors to an internal register which corresponds to an index value stored in said separate index register.

36. The system of claim 32, wherein the at least one module further includes:

a separate bank select register within the at least one module, corresponding to each of the at least two processors.

37. The system of claim 36, wherein said access control circuitry only allows access to said separate bank select register by said corresponding processor.

38. The system of claim 36, wherein the at least one module further includes at least one internal bank of registers; and

said access control circuitry only allows access by each of said at least two processors to an internal bank of registers indicated by the contents of said separate bank select register.

39. The system of claim 32, wherein the at least one module further includes at least one sub-element and ownership of said at least one sub-element is assigned to at least one of the at least two processors, and wherein said access control circuitry allows write access to said at least one sub-element only by said at least one of the at least two processors to which ownership is assigned.

40. A method for allowing concurrent access to at least one module by at least two processors including an embedded controller and a host processor; comprising the steps of:

receiving a transaction originating from one of the at least two processors;

receiving an indication of which of the at least two processors originated said transaction; and

processing said transaction within the at least one module based on said indication.

41. The method of claim 40, wherein said processing includes the step of:

directing at least part of said transaction to a sub-element of the at least one module, wherein said sub-element is owned by said processor which originated said transaction.

42. The method of claim 41, wherein said at least part of said transaction includes data.

43. The method of claim 40, wherein said processing includes the step of:

storing a data part of said transaction in at least one memory particular to said processor which originated said part of said transaction.

44. The method of claim 43, wherein said stored data part of said transaction indicates an index value of a register within the at least one module.

45. The method of claim 43, wherein said stored data part of said transaction indicates a bank of a register within the at least one module.

46. The method of claim 40, wherein said receiving of a transaction is at least partly via an internal bus whose clock differs based on which of the at least two processors originated said transaction.

47. A method for allowing shared access to at least one module by at least two processors including an embedded controller and a host processor, comprising the steps of:

blocking the access of at least one processor to the at least one module;

indicating to said at least one blocked processor that the at least one module is blocked; and

indicating to a processor which has blocked access to the at least one module if said at least one blocked processor has attempted access.

48. The method of claim 47, further comprising the step of:

said at least one blocked processor attempting to access the at least one module, prior to the step of indicating to said at least one blocked processor.

49. A method for allowing shared access to at least one module by at least two processors including an embedded controller and a host processor comprising the steps of:

blocking access by at least one processor to said at least one module; and

enabling said at least one module, as a result of the blocking step.

50. A method for allowing shared access to at least two modules by at least two processors including an embedded controller and a host processor, comprising the steps of:

receiving an indication from each of the at least two processors of a module from among the at least two modules to access;

arbitrating between the at least two processors in favor of one of the at least two processors; and

accessing said module indicated by said one of the at least two processors.

51. The method of claim 50, further comprising the step of:

blocking access by another of the at least two processors to said module indicated by said one of the at least two processors.

52. The method of claim 50, wherein said indication from each of the at least two processors is for a different module to access

53. A method for allowing an embedded controller to access at least two modules affiliated with a device, comprising the steps of:

indicating the device;

indicating an access direction (read/write);

indicating one of the at least two modules for accessing;

indicating a location for accessing, within said indicated one of the at least two modules; and

transferring data between said indicated location and the embedded controller.

54. The method of claim 53, wherein said indicated one of the at least two modules is accessible via a bus extension.

55. The method of claim 54, wherein said step of indicating one of the at least two modules for accessing includes the step of:

indicating one of at least one chip select corresponding to said bus extension for accessing.

56. The method of claim 53, wherein said indicated one of the at least two modules is part of an input/output chip.

57. The method of claim 56, wherein said step of indicating one of the at least two modules for accessing includes the step of:

indicating a logical device number.

58. The method of claim 53, wherein said step of indicating a location for accessing includes the step of providing an indication of a location for accessing via an internal bus to said indicated one of said at least two modules, the method further comprising the step of:

waiting for the freeing up of said internal bus before transferring said indication of a location for accessing onto said internal bus.

59. The method of claim 58, wherein said internal bus is occupied by a transaction originating from another processor prior to said freeing up.

60. The method of claim 53, further comprising the step of:

the controller waiting for receipt of data from said indicated location prior to initiating a subsequent access.

61. A method for preventing access by any of at least two processors including an embedded controller and a host processor to at least part of at least one module powered by a main power supply, when the main power supply is off, comprising the steps of:

determining that the main power supply is off;

indicating that the main power supply is off; and

preventing access to the at least part powered by the main power supply.

62. The method of claim 61, wherein said indicating is provided to at least one of the at least two processors whose interface is powered by a power source other than the main power supply.

63. The method of claim 62, wherein said indicating is provided to said at least one processor whose interface is powered by a power source other than the main power supply if said one processor attempts access to the at least part powered by the main power supply.

64. A system for increasing throughput to at least one module whose access is shared by at least two processors including an embedded controller and a host processor, comprising:

at least one module;

said at least one module using a clock when processing a transaction which differs based on which of the at least two processors originated said transaction.

65. The system of claim 64, further comprising a bus extension, wherein said at least one module is accessed via said bus extension.

66. The system of claim 64, wherein said at least one module is part of an input/output chip.

67. The system of claim 64, further comprising an internal bus for transferring a transaction originated by one of the at least two processors to said at least one module, wherein said internal bus has a clock which differs based on which of the at least two processors originated said transaction.

68. A method for increasing throughput to at least one module whose access is shared by at least two processors including an embedded controller and a host processor, comprising the steps of:

receiving a transaction from one of the at least two processors; and

processing said transaction by the at least one module using a different clock depending on which of the at least two processors originated said transaction.